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November 10, 1998

BOX PATENT APPLICATION
Assistant Commissioner for Patents
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Dear Sir:

Transmitted herewith for filing in the United States Patent and Trademark Office is the patent application of:

Inventor(s):	Douglas M. Albert, a citizen of the United States, and Volkon H. Ozguz, a citizen of Turkey
Docket No.:	IRV1.PAU.30
For:	METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME

Enclosed are a specification and claims (23 pages); a Declaration and Power of Attorney; a Declaration of Inventor(s) Claiming Small Entity Status; Two (2) sheets of drawings; a Declaration of Assignee Claiming Small Entity Status; an Assignment with Recordation Form Cover Sheet; a check in the amount of $40.00; a Certificate of Express Mailing; and this transmittal letter +1cc.

Respectfully submitted,

Joseph C. Andras
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JCA/erh

Enclosures

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METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME

Background of the Invention

Related Applications

The present application is a continuation in part of provisional patent application 60/065,088, filed Nov. 11, 1997, entitled "Method for Thinning Semiconductor Wafers with Circuits."

1. Field of the Invention

The field of endeavor of the invention relates to a method of thinning a semiconductor layer containing electronic circuits and the wafers made by such a method.

2. Description of the Prior Art

Silicon wafer thinning has been practiced in packaging technologies to reduce package thickness or to provide for a limited degree of flexibility for use in flexible electronic cards or smart cards. Examples of such manufacturing methods can be seen in **Flesher, et al.,** *"Flexible Electronic Card and Method,"* U.S. Patent 5,733,814 (1998). **Flesher**, however, is typical of the prior art processes wherein the backside of the wafer is mechanically ground before dicing the wafer to extract the semiconductor devices which are fabricated in the front side. Typically, the grinding process induces stresses in the wafer causing it to warp. The warped wafers are more likely to break during dicing as well as to

disintegrate or fracture during the grinding process itself. Warped and stressed dice are also more difficult to mount and are prone to break and shatter when flexed. Therefore, the level of thinning that can be achieved is limited. **Flesher** describes a modification of a mounting process to allow for back grinding, but still dices the wafers after the grinding and polishing of the back side of the wafer has been completed. The minimum thickness of the wafers reported in **Flesher** still exceeds 200 microns thick even for the thinnest wafers manufacturable according to **Flesher's** process. While dies made by **Flesher's** method may be suited for use within thick packages or a unreinforced credit card which is subject to only slight bending, wafers of this thickness are still too thick and friable to be mounted on flexible film.

Another prior art method for thinning wafers involves various types of methods for chemically etching away the back of the wafer such as described by **Clifton, et al.,** *"Method for Fabricating Thin, Strong, Flexible Die for Smart Cards,"* U.S. Patent 5,480,842 (1996) and **Edwards, et al.,** *"Manufacture of Thinned Substrate Imagers,"* U.S. Patent 4, 266,334 (1981). Chemical etching processes are more difficult to control in that the front surface of the wafer which includes the integrated circuits must be protected from the etchant. It is also difficult to determine exactly when the etching process ought to be stopped and to uniformly stop the etching process across the back of the wafer at very thin wafer thickness. Any imperfections or pin holes in the wafer may result in leakage of the etchant to the front surface and resulting in loss of yield.

Therefore, what is needed is some type of methodology whereby integrated circuit silicon wafers may be thinned to 50 microns or less thickness and less without undue concern for breakage. Only when the thickness of the wafer is reduced to 50 microns or less is it realistic to expect to obtain the

mechanical advantages of such flexibility and to obtain the thermal advantages of higher heat dissipation rates.

Brief Summary of the Invention

The invention is a method for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface. Typically, the wafer has a plurality of integrated circuits conventionally prefabricated in its front side. The circuits are organized into regions or dies which are separated by die streets which have been pre-scribed on the wafer. The method comprises the steps of defining a plurality of grooves into the die streets in the front side of the wafer. The grooves are allowed to penetrate into the surface by a predetermined distance which is less than the thickness of the semiconductor wafer so that the plurality of dies remain integral with the wafer. The grooves have a predetermined depth designed to provide stress relief in the following grinding step, which depth is equal to or greater than the final thickness of the thinned dies. The grooved wafer is mounted face down onto a flat rigid substrate which supports the wafer, i.e. the front side toward the substrate. The wafer is mounted to the substrate with the front surface turned toward the substrate. A predetermined portion of the backside of the wafer is mechanically removed until the thickness of the wafer is reduced to expose the plurality of grooves from the backside in preparation to separating the plurality of the dies. The dies remain mounted to the substrate. The plurality of dies are then released from the substrate.

The method further comprises the step of disposing a planarizing layer of low stress material on the front surface of the wafer into which the plurality of

grooves have been defined prior to defining the grooves into the front surface of the wafer.

The method further comprises the step of disposing a layer of low stress, low viscosity adhesive material on the front surface of the wafer into which the plurality of grooves have been defined prior to mounting the front surface of the wafer to the flat substrate. The step of mounting the flat substrate to the front surface of the wafer comprises affixing an optically flat substrate to the front surface of the wafer. The substrate has vertical variations of approximately one micron or less across its horizontal surface.

The method comprises in particular the step of disposing a polyimide layer on the front surface before the grooves had been defined therein and prior to mounting to the flat substrate, so that the polyimide layer absorbs stress induced into the wafer when mechanically removing a portion of the wafer.

The step of defining the plurality of the grooves in the wafer comprises defining grooves approximately 25 - 50 microns or less into the front surface of the wafer. The step of mechanically removing a portion of the wafer removes the backside portion of the wafer until the wafer has a thickness of 50 microns or less.

The step of releasing the plurality of dies comprises disposing the thinned backside surface of the wafer onto a pin block and dissolving the adhesive layer, thereby leaving the plurality of separated polyimide-coated dies on the pin block.

After the dies are separated, the method further comprises mounting the dies onto a flexible film and sealing the die mounted on the flexible film. The integrated circuit in the die is coupled to metalizations provided on the film. The die is disposed with the front surface in contact with the metalizations on the film and coupled thereto by means of anisotropic conductive epoxy.

The step of mounting the wafer to the substrate comprises affixing the front surface of the wafer to substrate on a surface of the substrate provided with a plurality of grooves defined in the substrate to facilitate the flow of adhesive material across the surface of the substrate between the surface of the substrate and the front surface of the wafer. The wafer and substrate are pressed together with a low viscosity and low stress material therebetween and the material cured while the pressure is maintained between the wafer and substrate.

The step of mechanically removing the wafer comprises grinding the backside portion of the wafer with at least one cycle of a predetermined grinding advance rate followed by a nonadvancing dwell. The grinding cycle is repeated two or more times with at least one reduction in the advance rate. If desired, the method further comprises the step of polishing the thinned backside surface of the wafer by a dry chemical etch having an etch rate of less than one micron per minute.

The invention can also be characterized as an intermediate work product produced in a manufacturing process of thinning dies. The intermediate product is an assembly used for manufacturing a plurality of flexible integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface. The assembly comprises a plurality of grooves defined into the front surface of the semiconductor wafer to define the plurality of dies. The grooves penetrate into the front surface a predetermined distance which is less than the thickness of the semiconductor wafer so that the plurality of dies remain integral with the wafer. A flat rigid substrate is mounted to the wafer to support the wafer. The wafer is mounted to the substrate with the front surface turned toward the substrate and to expose the backside of the wafer for partial mechanical removal of the backside by an amount sufficient to expose the

plurality of grooves to the backside in preparation to separating the plurality of the dies. The dies remain mounted to the substrate.

The invention may be better visualized by now turning to the following drawings wherein like elements are referenced by like numerals.

Brief Description of the Drawings

Fig. 1 is a perspective view of a glass substrate used in the method of the invention to support the wafer as it is thinned.

Fig. 2 is a side cross-sectional view in enlarged scale of a portion of a wafer showing the stress-relief grooves defined into the front surface.

Fig. 3 is a side elevational view of a wafer of Fig. 2 mounted on the substrate of Fig. 1 to form an assembly, which can be used for holding the wafer as its back side is ground.

Fig. 4 is a side cross-sectional view of the assembly of Fig. 3 after grinding showing the detachment of the thinned wafer from the substrate of Fig. 1.

Fig. 5 is a side cross-sectional of the thinned wafer obtained by the method of the invention shown mounted on a flexible film.

The invention and its various embodiments may now be better understood by turning to the following detailed description which is set forth as an illustration and not by way of limitation.

Detailed Description of the Preferred Embodiments

A conventional silicon wafer, having integrated circuits formed into its upper surface, can be successfully thinned to 50 microns or less using a

conventional, mechanical grinding apparatus, if performed by the method of the present invention. Prior to grinding, wafer is partially grooved or scored to create scribed grooves to a depth at least as deep or deeper than the final thickness desired in the thinned wafer. The grooves in the front surface provide stress relief and/or barriers to cracking. Any cracks or stress built up during the mechanical grinding operation, should they occur, propagate only to the edge of the nearest die street where the stress is relieved by breakage or crack termination.

As will be described below in greater detail, the silicon wafer is mounted on grooved or scored optically flat glass substrate with the front surface of the wafer bonded to the flat glass substrate using low viscosity, low stress bonding materials, such as a low stress adhesive. The thickness of the substrate bonding material and the surface variations of substrate is within plus or minus 0.1 micron. The use of the bonding materials eliminates affects arising from the nonuniformity of the surface topology of the integrated circuits of the silicon wafer.

The back surface of the silicon wafer is then ground according to the methodology described in greater detail below. The wafer is then thinned to 50 microns thickness or less by grinding down the back side of the mounted wafer. The grooves are ultimately exposed to result in an automatic separation of the dies mounted on the substrate. The polyimide layer disposed on the front surface of wafer also provides stress relief.

What results is a thinned integrated circuit chips fabricated by defining a plurality of grooves into the surface of a semiconductor wafer into which the integrated circuits are defined. The grid of grooves isolates each integrated

circuit into a separate chip or die. In the invention the grooves are extended only partially into the silicon, typically 50 microns by using conventional dicing or chemomechanical methods. The grooved wafer is then coated with a planarizing and stress relieving layer on the front surface of the wafer, which is that side of the wafer into which the circuits have been fabricated. The coated front surface wafer is then bonded with a low stress adhesive under pressure and at a curing temperature to the scored surface of an optically flat glass substrate. The substrate and bonded wafer thereby form a rigid and well supported assembly with the backside of the wafer exposed. The assembly is then mounted into a grinder which removes the backside portion of the wafer. When the grooves are exposed, the dies are separated while remaining affixed to the glass substrate. Grinding is achieved by advancing at a decreasing grind rate followed by periods of dwell wherein advancement is stopped in order to enhance stress relief. The grooves in the semiconductor wafer tend to inhibit stress buildup, crack formation and when cracks do occur they propagate to the die street limitations and are thus confined to a single die. The assembly is then placed on a pin block in a solvent with the thin backside disposed on the pin block. The solvent dissolves the adhesive layers leaving the separated dies of the pin block for mounting on a flexible film.

In one application the dies may be coupled to metalizations on the flexible film by means of a conductive epoxy and sealed using a flexible coating.

Turn now to the prospective view of Fig. 1 wherein the grooved, optically flat substrate 10 used in the methodology of the invention is shown in perspective view. Substrate 10 is formed of an optically flat glass disc of thickness 12, typically in the range of 0.5 to 1.5 cm. Upper surface 14 of substrate 10 is prepared so that it is optically flat, typically plus or minus 0.1 micron in variation from any one point on surface 14 to any other point. It must

be understood that the degree of optically flatness is described relative to the wavelength of light and may vary widely and still be included with the scope of the invention. For example, optically flat includes surfaces in which the surface variations may be constrained to the range of approximately $\lambda/2$ to $\lambda/20$ or flatter, where λ is the wavelength of light used as a standard of measurement. Opposing surface 16 (not visible in Fig. 1) is similarly prepared to be parallel and optically flat to surface 14. Substrate 10 is rigid and has a diameter sufficient to allow the mounting of a silicon wafer 20 (not shown in Fig. 1) to be mounted on surface 14.

Surface 14 of substrate 10 is then provided with a rectangular grid of grooves 18 formed by conventional scoring methods, e.g. either by dicing or photolithographic etching. The groove depth and center to center spacing of grooves 18 is variable and the illustrated embodiment groove depth is in the range of 75 to 125 microns with a groove width of 125 to 250 microns. Grooves are spaced apart from each other on 1,250 micron centers. These numerical examples are choosing only for illustration and any other shape, dimension or spacing may be used in the invention as may be desired and expedient. Grooves 18 run across the entire surface 14 with a second set of orthogonal grooves perpendicular to the first set to create a grid or checkerboard pattern. The topology of grooves 18, their thickness and spacing is not critical to the invention provided that grooves 18 provide a means wherein a low viscosity low stress bonding material later disposed on surface 14 is free to propagate or flow on surface 14 as facilitated by grooves 18 to form a layer of uniform thickness.

Fig. 2 is a side cross-sectional view of wafer 20 in which front surface 24 of wafer 20 has been partially diced to form a plurality of grooves 30 into surface 24. Grooves 30 define dies 34 in surface 24 in which the integrated circuit has

been formed. Thus, each die 34 will ultimately form a separate integrated circuit chip. Grooves 30 have a depth 32 equal to or slightly exceeding the final thickness desired for wafer 20 after thinning. For example, grooves 30 in the illustrated embodiment have a depth 32 in the range of 10 to 75 microns. The total thickness 36 of wafer 20 before thinning typically is in the range of 500 to 1000 microns. The pattern formed by grooves 30 is thus dictated by the chip size and geometry and is otherwise conventional. Die street 30 may be created by any method now known or later devised, such as photolithographic etching or mechanical grinding with a diamond saw wheel. Surface 24 is provided first with a polyimide layer 26 and then partial diced to create grooves 30 on surface 24, and then an adhesive layer 28 as described below in connection with Fig. 3 is disposed on the grooved polyimide-coated surface 24.

Thus, grooves 30 form a grid of trenches or grooves of about 25 to 50 microns in depth around each die 34 on front surface 24 of each die. Grooves 30 typically follow the streets of wafer 20 as manufactured as an integrated circuit wafer. Grooves 30 are made by photolithographic etchings or scribings. The use of a photolithographic etch will allow the formation of die 34 with smooth edges and will tend to eliminate chipping or cracking that may result from a standard wheel based dicing. As will be described below, wafer 20 is then thinned to 25 microns from backside 22 and grooves 30 will be exposed to automatically separate dies 34 on wafer 20 when released from substrate 10. The photolithographic accuracy obtained during dicing can then later be used to position the die within a stack of dies or on a flexible substrate. Furthermore, formation grooves 30 act as a means for stress relief during thinning of wafer 20 by eliminating crack formation, or, if a crack is formed, by restricting its propagation within a single die boundary.

Fig. 3 is a side cross-sectional view of substrate 10 shown mounted to silicon wafer 20. Backside 22 of silicon wafer is exposed while its front surface 24 is coated with a polyimide layer 26. The thickness of polyimide layer 26 is approximately 4 to 8 microns and is disposed on surface 24 on wafer 20 by spinning, spraying or film forming. The function of polyimide layer 26 is to provide a degree of planarization for the front surface 24 of wafer 20 and to act as a stress relieving layer. An adhesive layer 28 of approximately 10 microns thickness is disposed on polyimide layer 24 by spraying or spinning. Wafer 20 is then mounted on surface 14 of substrate 10 using a press at a regulated pressure and temperature. For example, pressure on a 6 inch diameter wafer 20 of about 70 psi applied for about 5 minutes at about 23°C forces the assembly 38 of Fig. 3 together so as to spread and cure adhesive layer 28 in order to provide a secure bond of wafer 22 substrate 10 with a uniform thickness. Any excess bonding material squeezed out from between wafer 20 and substrate 10 can then be manually removed with a razor blade. Grooves 18 in substrate 10 provide a means whereby adhesive 28 and polyimide layer 24 may flow and be distributed across surface 14 so that backside surface 22 of wafer 20 is parallel to surfaces 14 and 16 of substrate 10 in preparation for the following grinding operation.

After wafer 20 is securely mounted to substrate 10 as described in connection with Fig. 3, assembly 38 of Fig. 3 is then placed into a conventional mechanical grinding machine, such as Model 7AA manufactured by R.H.Strausbaugh of San Luis Obispo, California. A course grind is first performed on backside 22 at a rate of about 3 microns per second until reaching the desired set point using a 40/60 micron diamond grit wheel at about 2500 rpm. The grinding rate is then slowed to about 1 micron per second for the next

10 microns of grind. The grinding wheel is then held in a stationary or dwell position for about 10 seconds, which has been found according to the invention to further provides stress relief. At approximately 20 microns above the final, desire thickness, thin backside 22 is then ground or polished with a finer grinding wheel, such as 4/6 micron grit diamond wheel at 4350 rpm. The final grinding cycles are again performed at predetermined advance rates followed by dwell times until the final wafer thickness 36 of 50 microns or less is obtained. Again the numerical examples have been set forth only to illustrate the invention, which is not to be taken as limited by the numerical example given. For example, the grinding rates, wheel speeds and grits may change if a different wafer grinder is used.

Assembly 38 of Fig. 3 is then removed from the grinding machine and wafer 20 demounted. Wafer 20 is demounted by immersing assembly 38 into a solvent, such as acetone which serves to dissolve adhesive layer 28 as shown in Fig. 4. Grooves 30 may be partially or completely filled with adhesive layer 28 which is dissolved by warm solvent 40. Assembly 38 is placed upon a pin block 42 which is provided with a plurality of pins or apexes 44 on its upper surface so that the backside layer 22 of thin wafer 20 is in contact with pin block 42 only in a plurality of small areal points. This prevents any substantial liquid surface tension from being created between dies 34 and pin block 42. If surface tension had been allowed to develop between pin block 42 and die 34, thinness of dies 34 is such that any attempt to remove die 34 from pin block 42 would subject die 34 to substantial stresses resulting in a high probability of breakage.

Solvent 40 dissolves away adhesive layer 28 from substrate 10, which can then be gently shaken to separate the plurality of dies 34 from substrate 10. Dies 34 are then left, each separated from the other in their original position on

points 44 of pin block 42. Dies 34 are then individually removed from pin block 42 using vacuum tweezers or other means and placed in chip carriers and handled or processed in a conventional manner.

Thus, it may be appreciated that a backside dry or wet etching is avoided in the present invention to eliminate the damage to the circuits in front side 24. Dry etching from backside 22 of wafer 20 may create defects due to the close proximity of the active layers and front surface 24. Wet etching of backside 24 leaves etch pits and enhances the propagation of microcracks. Nevertheless, a final touch up chemical etch with a very slow silicon etch of less than one micron per minute may optionally be used in some cases.

The thin flexible dies 34 are attached to conventional Kapton cable and interconnected to the cable using metal depositions. Kapton film 46 in Fig. 5 is conventional 25 micron thick film using quarter ounce laminated substrates. Single dies 34 mounted on film 46 are capable of flexing to radii of curvature of less than 20 millimeters without breaking. Multiple numbers of the thinned die 34 may be stacked by providing additional passivation layers on dies 34 and metalizations on top of die 34. Lead connections to dies 34 are provided on the side of die 34, which result in pad pitches as low as 3 mils.

The thinnest dies 34 also allow for clear visualization of circuit layers in die 34 thereby creating an opportunity for optical quality control of the multiple layers of the finished die. The opaque metalizations are clearly delineated against the illuminated translucent silicon when die 34 is back lit.

Thin die 34 can be electrically connected to flexible Kapton carrier using z-bonding as shown in Fig. 5. Die 34 is bonded to Kapton film 46 through the use of a z-conductive epoxy 48. Z-conductive epoxy is preferred because it

allows the die-to-substrate connection process to be simplified and the adhesive properties of the epoxy support die 34. In the illustrated embodiment, thermoplastic z-conductive adhesive manufactured by A.I. Technologies under the part no. ZSP8150-FP has been used. This particular epoxy can support line pitches in the range of 2 - 6 mils. When cured, its thickness is less than 0.5 mils and is characterized as a film. Because thin die 34, z-conductive epoxy 48 and Kapton film 46 are all transparent, die 34 can be easily aligned so that its circuit metalizations 50 are matched with conforming metalizations 52 on the opposing surface 54 of Kapton film 46.

Mounted die 34 in Fig. 4 is then sealed on Kapton film 46 using a flexible seal such as additionally adhesively disposed Kapton layers or sprayed coatings. Alternatively, different materials may be chosen for film 46. Inorganic coatings which are deposited, sprayed, sputtered or evaporated on to film 46 and die 34 are also possible as seals.

In the very early runs of the present invention, demonstrations have been made whereby dies with a final thickness of 35 microns can be recovered with yields in excess of 80% by utilizing the above methodology in six inch wafers. Similar yields have been obtained with dies of 25 microns of thickness and 5 inch silicon wafers with the integrated circuits still electrically functioning.

With circuit die 34 having a thickness of 50 microns or less, circuits can be mounted on flexible plastic films and bent into nonplanar shapes without significant danger of fracture. Thin circuit chips devised according to the invention can tolerate more stress in packaging and in operation because of this flexibility. The minimum mass in die 34 results in a mechanical stability of the integrated circuit under high acceleration loads and shocks. High frequency

electrical performance of the circuit is also enhanced, since parasitic capacitance in the substrate is reduced or eliminated. Radiation tolerance of the circuit is also improved, since the carrier generation volume is minimized. The flexibility of circuits is exploited where space is a premium and odd shapes need to be obtained such as in rollup displays, wrist worn electronic products, shaped conforming sensors and flexible smart cards.

Many alterations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention. Therefore, it must be understood that the illustrated embodiment has been set forth only for the purposes of example and that it should not be taken as limiting the invention as defined by the following claims.

The words used in this specification to describe the invention and its various embodiments are to be understood not only in the sense of their commonly defined meanings, but to include by special definition in this specification structure, material or acts beyond the scope of the commonly defined meanings. Thus if an element can be understood in the context of this specification as including more than one meaning, then its use in a claim must be understood as being generic to all possible meanings supported by the specification and by the word itself.

The definitions of the words or elements of the following claims are, therefore, defined in this specification to include not only the combination of elements which are literally set forth, but all equivalent structure, material or acts for performing substantially the same function in substantially the same way to obtain substantially the same result. In this sense it is therefore contemplated that an equivalent substitution of two or more elements may be made for any

one of the elements in the claims below or that a single element may be substituted for two or more elements in a claim.

Insubstantial changes from the claimed subject matter as viewed by a person with ordinary skill in the art, now known or later devised, are expressly contemplated as being equivalently within the scope of the claims. Therefore, obvious substitutions now or later known to one with ordinary skill in the art are defined to be within the scope of the defined elements.

The claims are thus to be understood to include what is specifically illustrated and described above, what is conceptionally equivalent, what can be obviously substituted and also what essentially incorporates the essential idea of the invention.

We claim:

1. A method for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising:

defining a plurality of grooves into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said surface at a predetermined distance less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer;

mounting said wafer to a flat rigid substrate to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate;

mechanically removing a predetermined portion of said backside of said wafer until said thickness of said wafer is reduced to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining of mounted to said substrate; and

releasing said plurality of dies from said substrate.

2. The method of claim 1 further comprising disposing a planarizing layer of low stress material on said front surface of said wafer into which said plurality of grooves have been defined prior to mounting said front surface of said wafer to said flat substrate.

3. The method of claim 1 further comprising disposing a layer of low stress material on said front surface of said wafer before defining said plurality of grooves into said front surface of said wafer.

4. The method of claim 1 where mounting said flat substrate to said front surface of said wafer comprises affixing an optically flat substrate to said front surface of said wafer.

5. The method of claim 4 where affixing said optically flat substrate comprises affixing said front surface of said wafer to a surface of said substrate which has vertical variations of approximately one micron or less across said surface.

6. The method of claim 1 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to mounting to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when mechanically removing a portion of said wafer.

7. The method of claim 1 wherein defining said plurality of said grooves in said wafer comprises defining grooves approximately 50 microns deep into said front surface of said wafer.

8. The method of claim 7 wherein mechanically removing a portion of said wafer removes said backside portion of said wafer until said wafer has a thickness of 50 microns or less.

9. The method of claim 8 wherein mechanically removing a portion of said wafer removes said backside portion of said wafer until said wafer has a thickness of approximately 25 microns or less.

10. The method of claim 1 wherein mounting said wafer to said flat substrate comprises affixing said wafer by means of a low viscosity low stress adhesive.

11. The method of claim 10 further comprising disposing a polyimide layer on said front surface before said grooves are defined therein and prior to affixing to said flat substrate, so that said polyimide layer absorbs stress induced into said wafer when said grooves are mechanically formed in said wafer.

12. The method of claim 11 where releasing said plurality of dies comprises disposing said thinned backside surface of said wafer onto a pin block and dissolving said adhesive layer, thereby leaving said plurality of separated dies on said pin block.

13. The method of claim 1 further comprising mounting said dies onto a flexible film.

14. The method of claim 13 further comprising sealing said die mounted on said flexible film.

15. The method of claim 13 where mounting said die on said flexible film further comprises electrically coupling said integrated circuit in said die to metalizations provided on said film.

16. The method of claim 15 where electrically coupling said integrated circuit on said die to metalizations on said film comprises disposing said die with said front surface in contact with said metalizations on said film and coupled thereto by means of conductive epoxy.

17. The method of claim 1 where mounting said wafer to said substrate comprises affixing said front surface of said wafer to substrate on a surface of said substrate provided with a plurality of grooves defined in said substrate to facilitate the flow of material across said surface of said substrate between said surface of said substrate and said front surface of said wafer.

18. The method of claim 17 wherein affixing said front surface to said flat substrate comprises affixing said front surface using low viscosity, low stress materials disposed between said front surface and said flat substrate.

19. The method of claim 18 further comprising pressing said wafer and substrate together with said low viscosity and low stress material therebetween

and curing said material while maintaining said pressure between said wafer and substrate.

20. The method of claim 1 where mechanically removing said wafer comprises grinding said backside portion of said wafer with at least one cycle of a predetermined grinding advance rate followed by a nonadvancing dwell.

21. The method of claim 20 where grinding with a least one advance rate and dwell comprises at least one reduction in said advance rate.

22. The method of claim 21 further comprising polishing said thinned backside surface of said wafer by a dry chemical etch having an etch rate of less than one micron per minute or a mechanical polish having an advance rate of less than one micron per minute.

23. The method of claim 1 where defining said plurality of grooves in said front surface of said wafer comprises defining linear grooves into said front surface of said wafer in an intersecting grid pattern to define each of said dies, thereby isolating each die by a surrounding moat of stress relieving grooves.

24. The method of claim 1 further comprising stacking a plurality of separated dies prepared by said method, and electrically interconnecting said dies.

25. An assembly used for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising:

a plurality of grooves defined into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said front surface a predetermined distance which is less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer; and

a flat rigid substrate mounted to said wafer to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate and to expose said backside of said wafer for partial mechanical removal of said backside by an amount sufficient to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining of mounted to said substrate.

26. The assembly of claim 25 further comprising a low viscosity, low stress layer disposed between said front surface of said wafer and said substrate to affix said front surface of said wafer to said substrate.

27. The assembly of claim 26 wherein said low viscosity, low stress layer includes a polyimide layer disposed on said front surface.

METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME

Abstract of the Disclosure

Thinned and/or flexible integrated circuit chips are fabricated by defining a plurality of grooves into the front surface of a semiconductor wafer. The grooves isolate each integrated circuit into a separate die. The pre-scribed grooves extend only partially into the front surface in which the circuits are formed, typically 50 microns or less. A polyimide planarizing and stress relieving layer is disposed on the front surface before the grooves are grooved. A low viscosity low stress adhesive is disposed on the grooved polyimide coated surface. The wafer is then bonded to the scored surface of an optically flat glass substrate under pressure and at a curing temperature. The assembly is then mounted into a grinder which removes the backside portion of the wafer until the grooves are exposed. Grinding is achieved by advancing at a decreasing grind rate followed by periods of dwell. The grooves in the semiconductor wafer tend to inhibit crack formation and when cracks do occur they propagate to the die street limitations and are thus confined to a single die. The assembly is then placed backside down on a pin block in a solvent bath. The solvent dissolves the adhesive layer leaving the separated dies of the pin block for mounting on a flexible film. The dies are coupled to metalizations on the flexible film by means of a conductive epoxy and sealed using a flexible coating.

Fig. 1

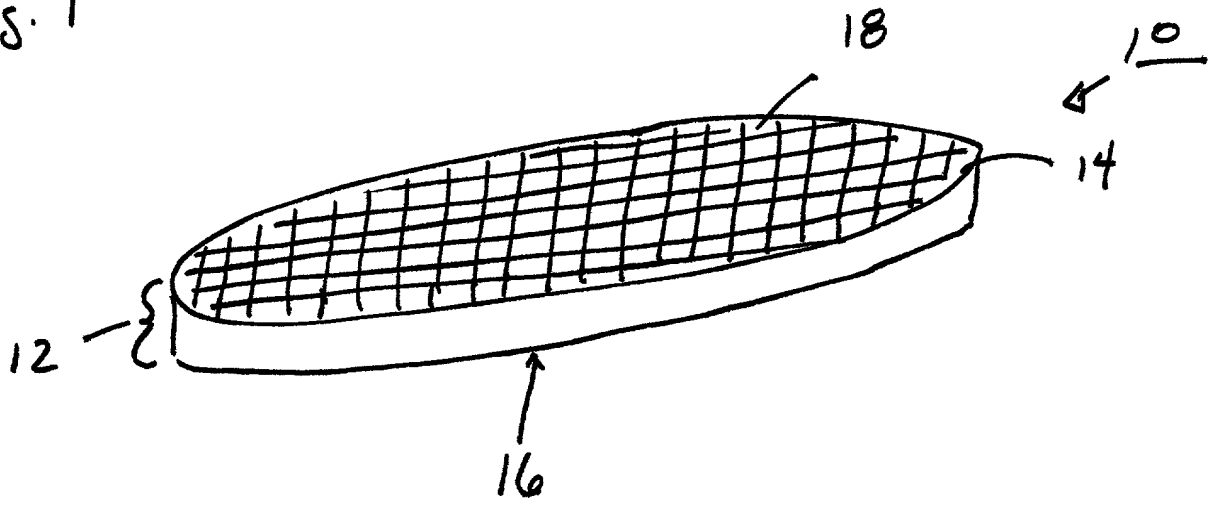


Fig. 2

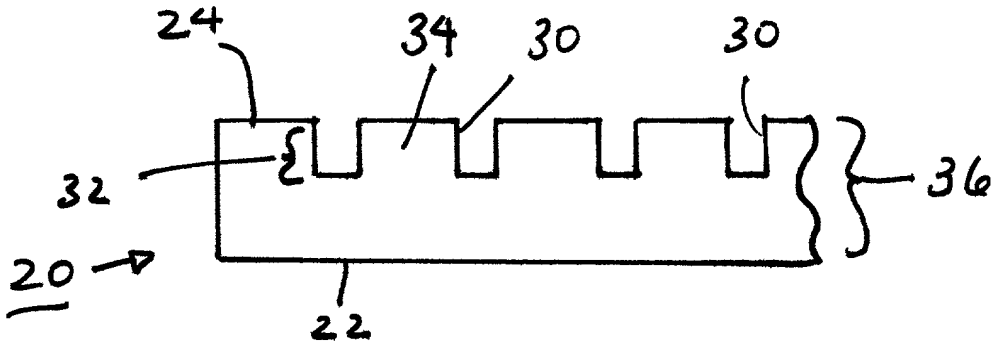


Fig. 3

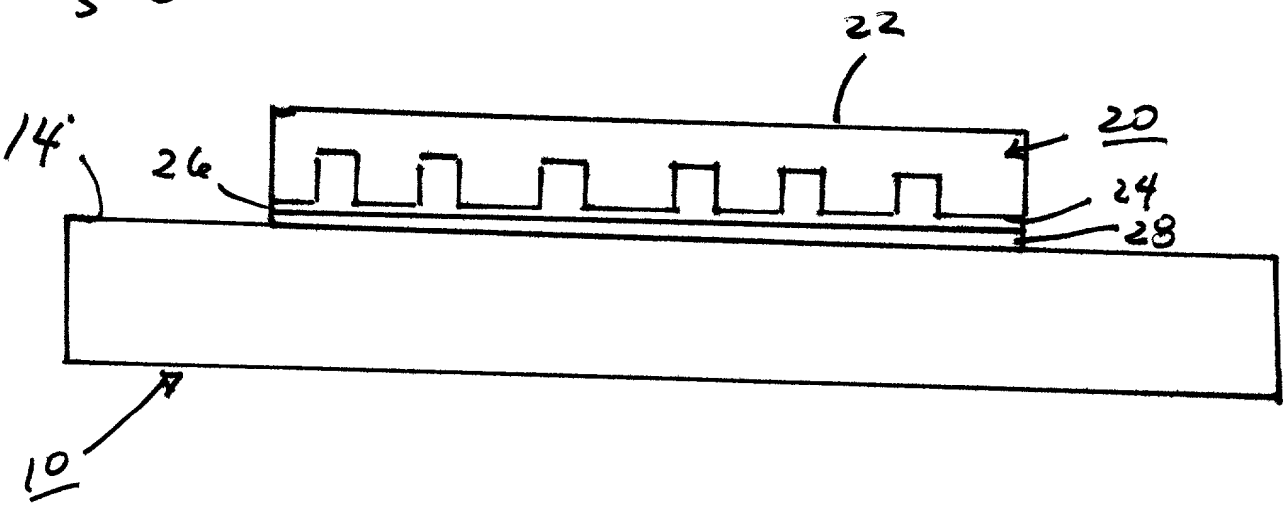


Fig. 4

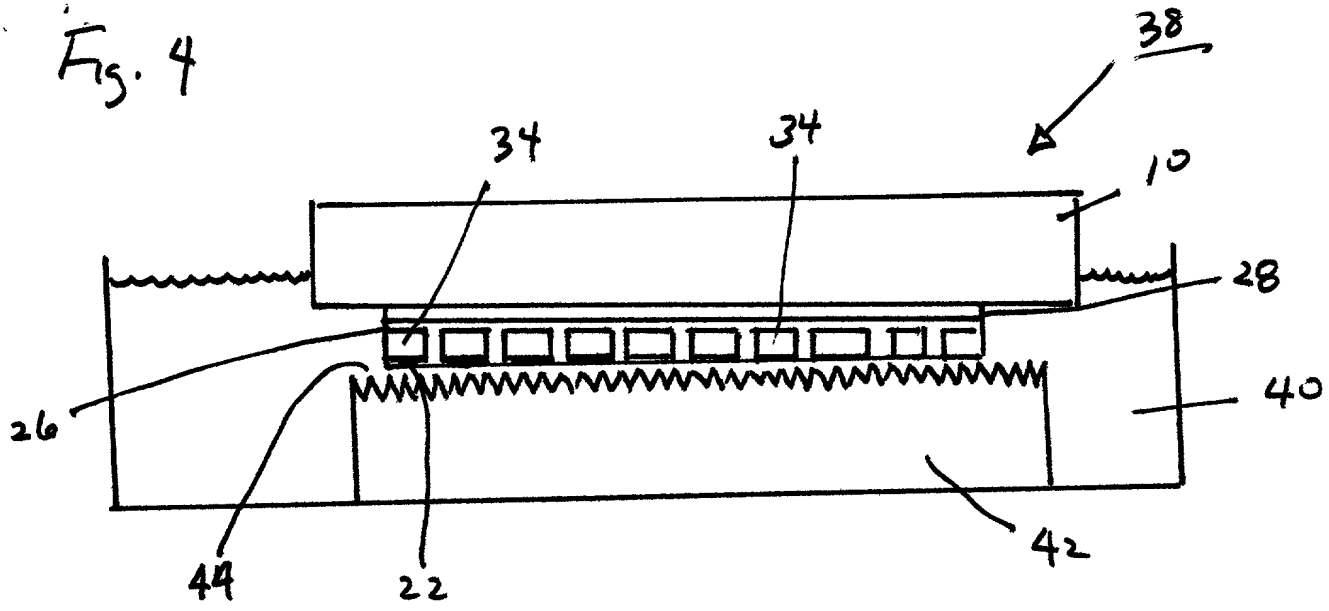
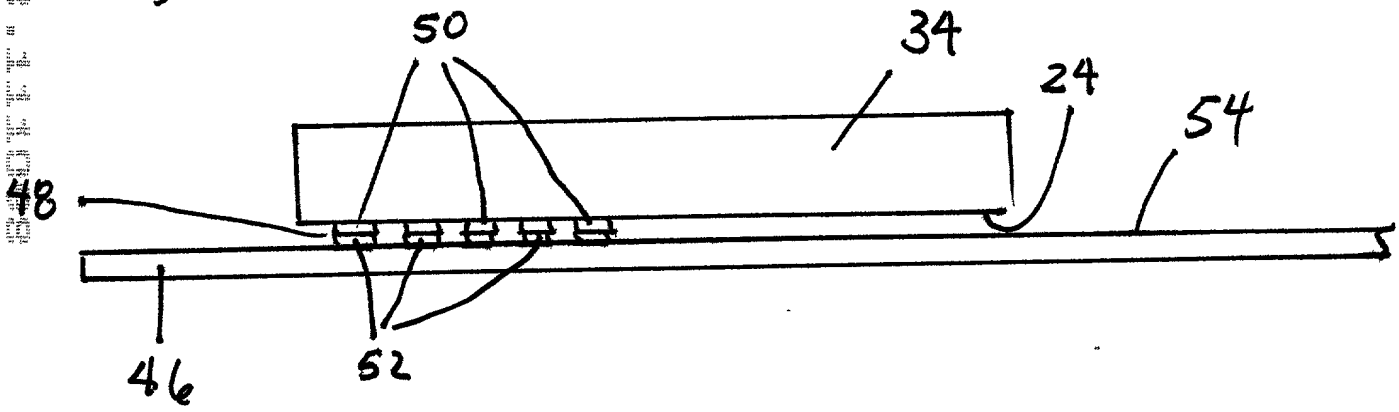


Fig. 5



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Douglas M. Albert et al.

Serial No.: Unknown

Filed: Herewith

Titled: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME

DECLARATION OF ASSIGNEE CLAIMING SMALL ENTITY STATUS

As an assignee in and to the above identified invention and application, I hereby declare that I qualify as an assignee as defined in 37 CFR 1.9 (c) and (d), for purposes of paying reduced fees under Sections 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention set forth in the application identified above.

I have not assigned, granted, conveyed or licensed, and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted conveyed or licensed, or am under an obligation under contract or law to assign, grant , convey, or license, any rights in the invention are identified as follows:

NONE

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or

imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Assignee: **Irvine Sensors Corporation**
3001 Redhill Avenue
Building 3, Suite 104
Costa Mesa, California 92626

November 10, 1998
Date

By: John Carson,
Senior Vice-President

As a below named inventor of the invention claimed in the below application for United States Letters Patent, I hereby declare that:

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the invention which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME

the specification of which was filed of even date herewith.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby sate that I have reviewed and understand the contents of the above application, including the specification and claims thereof, and acknowledge my duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

PRIORITY CLAIMS

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate, or of any PCT international application(s) designating at least one country other than the United States of America, filed by me on the same subject matter as set forth in the attached application, namely:

- NONE

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

- U.S. Provisional Application Serial No. 60/065,088, filed November 11, 1997.

I hereby claim the benefits under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, Untied States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

- NONE

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Joseph C. Andras Registration No. 33,469

Please send correspondence and direct telephone calls to:

Joseph C. Andras
LAW OFFICES OF JOSEPH C. ANDRAS
650 Town Center Drive, Suite 650
Costa Mesa, California 92626
(714) 759-4760

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF FIRST OR SOLE INVENTOR:

Full Name:	Douglas M. Albert
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Post Office Address:	17743 Plum Tree Lane Yorba Linda, California 92886
Residence:	Same as PO Address
Date:	11/10/98
Inventor's Signature:	Douglas M. Albert

SIGNATURE OF SECOND JOINT INVENTOR:

Full Name:	Volkan H. Ozguz
Citizenship:	Turkey
Post Office Address:	8 Palatine Aliso Viejo, California 92656
Residence:	Same as PO Address
Date:	11/10/98
Inventor's Signature:	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Douglas M. Albert et al.

Serial No.: Unknown

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Titled: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME

DECLARATION OF INVENTOR(S) CLAIMING SMALL ENTITY STATUS

As a below named inventor, I hereby declare that I qualify as an independent inventor, as defined in 37 CFR 1.9(c), for purposes of paying reduced fees under Sections 41(a) and (b) of Title 35, United States code, to the Patent and Trademark Office with regard to the invention set forth in the application identified above.

I have not assigned, granted, conveyed or licensed, and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted conveyed or licensed, or am under an obligation under contract or law to assign, grant , convey, or license, any rights in the invention are identified as follows:

IRVINE SENSORS CORPORATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or

imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Full Name of First or Sole Inventor: **Douglas M. Albert**

11/10/98
Date

Douglas M. Albert
Signature of First or Sole Inventor

Full Name of Second Joint Inventor **Volkan H. Ozguz**

11/10/98
Date

Volkan H. Ozguz
Signature of Second Joint Inventor